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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,289	12/28/2001	Young-Hun Ha	8733.560.00	2930

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EXAMINER	
DI GRAZIO, JEANNE A	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 10/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,289	HA ET AL.	
	Examiner	Art Unit	
	Jeanne A. Di Grazio	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

Priority to Korean Patent Application 2000-0085421 (Dec. 29, 2000) is claimed.

Interview Summary

The Examiner thanks Applicant's representative for having taken the time to clarify, by telephone interview on October 16, 2003, certain unclear aspects of the invention at issue.

Per telephone interview with Applicant's representative, Mr. George Baus, on Thursday, October 16, 2003, the Examiner and Mr. Baus discussed possible wording to clarify the language of claim 13. In particular, the last limitation, "a passivation layer removed where electric lines are not formed, the removal of the passivation layer maintaining cell gap distance between the display area and the seal pattern forming region" was discussed as being unclear. While possibilities for clarifying the claim language were discussed, no definite agreement was reached at that time.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 13 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation "a passivation layer removed where electric lines are not formed, the removal of the passivation layer maintaining cell gap distances between the display area and the seal pattern forming region" is unclear to one of ordinary skill in the art.

One of ordinary skill in the art would not appreciate the location of "where the electric lines are not formed" in relation to the passivation layer. One of ordinary skill would also not appreciate how the removal of a passivation layer maintains the cell spacing.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 6, 9, 10, and 12 rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki et al. (US 5,739,880).

Per claims 1, 2, 9, 10, and 12: Referring to Figure 5(a), Suzuki has a lower substrate (SUB1) including a seal pattern forming region (SL) between a display area and a non-display area of the lower substrate wherein a passivation layer (PSV1) is removed. As broadly interpreted, the passivation layer (PSV1) is removed in the seal pattern forming region according to Figure 5(a). Stated differently, the passivation layer is not a continuous layer; the passivation layer does not cover the entire seal pattern forming region. Therefore, the passivation layer is removed in this region. Suzuki furthermore has an upper substrate (SUB2). The seal pattern is formed in a boundary region between the display area and the non-display area of the lower substrate. A liquid crystal layer (LC) is between the substrates.

Per claim 3: Referring to Figure 5, The lower substrate (SUB1) includes a gate electrode (GT) on the first substrate, a gate insulating layer (GI) on the first substrate and on the gate

electrode, a thin film transistor on the gate insulating layer (TFT), a pixel electrode (ITO 1) that is connected to the thin film transistor on the gate insulating layer and a passivation layer (PSV1) on the thin film transistor.

Per claim 4: Referring to Figure 5, the upper substrate includes a second substrate (SUB2), a color filter (FIL(R) and FIL(G)), and a common electrode (ITO 2(COM)).

Per claim 6: Suzuki furthermore has numerous spacers for maintaining substrate gap (Col. 14, Lines 58-61).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5 and 20 rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (US 5,739,880) in view of Park et al. (US 6,621,545 B2).

Per claims 5 and 20: Suzuki does not appear to explicitly specify that the passivation layer is removed during a photolithographic mask step for simultaneously patterning an active layer and the passivation layer; however, Park has simultaneous etching of a passivation layer and semiconductor layer (Park, Claim 5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Suzuki in view of Park to reduce the number of process steps.

Claims 7, 8, 18, and 19 rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (US 5,739,880).

Per claims 7, 8, 18, and 19: Referring to Figure 5a, Suzuki has a lower substrate (SUB1) where a passivation layer (PSV1) is removed, an upper substrate (SUB2) including a color filter (FIL R & G) and a common electrode (ITO 2 COM), spacers between upper and lower substrates (Col. 14, Lines 57-61), a seal pattern (SL) in a boundary between display and non-display areas, the seal pattern contacts a gate insulating layer (g1), and liquid crystal injected into an interior of the seal pattern (Col. 15, Lines 1-3).

Suzuki furthermore has a gate electrode (GT) on the first substrate, a gate insulating layer (GI) on the first substrate and on the gate electrode, a thin film transistor on the gate insulating layer (TFT), a pixel electrode (ITO 1) that is connected to the thin film transistor on the gate insulating layer and a passivation layer (PSV1) on the thin film transistor.

Suzuki does not appear to explicitly disclose a fabricating method for forming the LCD panel; however, Suzuki has the device for improved adhesion.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to derive a method of fabricating the above display for improved adhesion.

Claim 11 rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki et al. (US 5,739,880) in view of Miyachi et al. (US 6,384,889 B1).

Per claim 11: Suzuki does not appear to explicitly specify that the seal pattern is formed by screen printing using thermosetting resin that includes glass fiber; however, Miyachi teaches a seal section formed of an epoxy resin including fiber glass and formed along a periphery of a display region by screen printing (Col. 19, Lines 65-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Suzuki in view of Miyachi for a seal having great mechanical strength and for adhesion.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lim et al. (US 6,448, 579 B1) in view of Aoki et al. (US 4,723,838), in view of Kohei et al. (JP 11-326949), in view of Ikeda (US 6,172,729 B1), in view of Nishiguchi et al. (US '553) and further in view of Bae (US 2002/0030769 A1).

Per claim 13: Lim et al. has a plurality of gate lines including a gate electrode and capacitor electrode on an array substrate (Col. 3, Lines 35, 61 and Col. 4, Lines 16-17). Lim also has a plurality of data lines including a drain electrode (Col. 3, Line 36 and Col. 4, Lines 5-6). The gate and data lines cross each other (Col. 3, Lines 36-37). Lim also has gate and data pads formed at one end of the gate and data lines (Col. 2, Lines 59-61). Lim also has source and drain electrodes spaced apart from each other (Figure 5c). Lim furthermore has a pixel electrode (135) partially overlapping with a first capacitor electrode (123)(referring to Figure 6a). Lim has a semiconductor layer (39) (Prior Art, Figures 2b and 2c) forming a semiconductor channel region (53) below source (45) and drain electrodes (47).

Lim does not appear to have the semiconductor layer under source and drain electrodes including the TFT including the gate electrode; however, Aoki has a semiconductor layer (21) formed underneath TFTs (16) and including the gate electrode (23) (referring to Figure 12 I) for prevention of contamination and for sufficient insulation.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lim in view of Aoki so that contamination of semiconductor layers can be prevented, sufficient insulation can be had between the source / drain and gate electrodes, high contrast, and to prevent breaking of elements in the structure (Aoki at Col. 3, Lines 40-62 et al.).

Lim does not appear to have an auxiliary capacitance electrode electrically connected to a pixel electrode; however, Kohei has a pixel electrode and auxiliary capacity electrode electrically connected to each other (PAJ) to reduce the number of process steps.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lim in view of Kohei to reduce the number of process steps as noted in Kohei (PAJ).

Lim does not appear to have the auxiliary capacitance electrode formed between the capacitance and pixel electrode; however, Ikeda has an auxiliary capacitance electrode between the capacitance electrode and the pixel electrode (Col. 1, Lines 50-62).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lim in view of Ikeda for a common storage type capacitor as noted in Ikeda (Id.).

Lim does not appear to have a seal pattern formed between a data pad and adjacent portion of a data line to assemble substrates with a uniform cell gap; however, Yamamoto et al. (US '460) has a sealant forming around a periphery of a drive circuit (Figure 6) to easily repair disconnection.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lim in view of Yamamoto for ease in repair of disconnection as noted in Yamamoto.

Lim does not appear to have a seal pattern dividing the array substrate into display and non-display regions; however, as noted, Nishiguchi has this limitation. Nishiguchi has each substrate that has a display and non-display section (Col. 3, Lines 61-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lim in view of Nishiguchi so that surfaces of the substrates on which electrodes are respectively formed face each other (Nishiguchi, Col. 3, Lines 61-65).

Lim does not appear to have a passivation layer removed in an area where electric lines are not formed; however, Bae has a passivation layer removed in the sealant region [0064] where the sealant region is on the boundary between display and non-display regions as noted.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lim in view of Bae for improved adhesion and uniform substrate gap.

Claims 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rho et al. (US '146 B1) in view of Hoffmann et al. (US '471) and further in view of Kataoka et al. (JP-10-090717).

Per claims 14-17: Rho has substrates and a spacer disposed between the substrates, a storage capacitor including a capacitance electrode formed on a transparent substrate (Col. 2, Lines 38-42), a gate insulating layer formed on the transparent substrate and on the capacitance electrode (Figure 4), and a semiconductor layer formed on the gate insulating layer / transparent substrate (Figure 4). Rho has a pixel electrode formed on a passivation layer (Figure 4).

Rho furthermore has a gate electrode on a transparent substrate, a gate insulating layer on the transparent substrate and on the gate electrode, and a source and drain electrode spaced apart from each other and formed on a semiconductor layer. Rho also has a semiconductor layer including an active layer and an ohmic contact layer where the semiconductor layer is formed on the gate insulating layer (Figure 4).

Rho does not appear to explicitly specify an auxiliary capacitance electrode formed on the semiconductor layer; however, Hoffmann has a storage capacitor and storage capacitor electrode arranged above a doped semiconductor layer [ABS.] for reduced array size.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Rho in view of Hoffmann for reduced size (area) of the array device as noted in Hoffmann.

Rho does not appear to have a pixel electrode contacting a lateral side of an auxiliary capacitance electrode; however, Kataoka has a pixel electrode (19) contacting a side of an auxiliary capacitor (4) (PAJ) for increased auxiliary capacity area without increasing auxiliary capacity area. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Rho in view of Kataoka for increased capacity without increased area.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeanne A. Di Grazio whose telephone number is (703)305-7009. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached on (703) 305-3492. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Jeanne Andrea Di Grazio

JDG

Robert Kim, SPE

TOAN TON
Primary Examiner
Tech Ctr 2800